Request for Proposals (RFP)

The provision for the design and production of a Transceiver Analogue Front End and High Speed Digital Data Capture System to CSIR

RFP No. 892/02/09/2019

Date of Issue	Friday, 16 August 2019	
Compulsory briefing session	Date: Friday, 23 August 2019 – details below Time: 10:00am Venue: CSIR – Meiring Naude Road Building 14E – SST Boardroom Brummeria Pretoria, 0184	
Closing Date	Monday, 02 September 2019	
Place	Tender box, CSIR Main Reception, Gate 3 (North Gate)	
Enquiries	Strategic Procurement Unit	E-mail: tender@csir.co.za
CSIR business hours	08h00 – 16h30	
Category	Professional services	

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SECTION A – TECHNICAL INFORMATION

1 INTRODUCTION

The Council for Scientific and Industrial Research (CSIR) is one of the leading scientific research and technology development organisations in Africa. In partnership with national and international research and technology institutions, CSIR undertakes directed and multidisciplinary research and technology innovation that contributes to the improvement of the quality of life of South Africans. The CSIR's main site is in Pretoria while it is represented in other provinces of South Africa through regional offices.

2 BACKGROUND

The CSIR has developed a number of specialized remote sensing and communication systems that operate between 5 kHz and 500 kHz. As part of a drive to improve system performance, there is a need to develop portable analogue front-end acquisition hardware which can be located in close proximity to the sensors. A transceiver analogue front-end and high-speed data capture system is therefore required which is capable of transmitting and receiving signals from 5 kHz to 500 kHz. The system must be able to repeatedly and synchronously (to within a tenth of a wavelength) synthesize digital transmit waveforms on at least 4 channels and acquire/sample data from at least 32 sensors. The system must on each transmit/receive cycle stream the acquired data to a host PC/laptop. Further details of the requirements of the system are specified below.

3 INVITATION FOR PROPOSAL

Proposals are hereby invited for the provision for the design and production of a Transceiver Analogue Front End and High Speed Digital Data Capture System to CSIR, a block diagram of the required solution is shown in Fig.1 below.

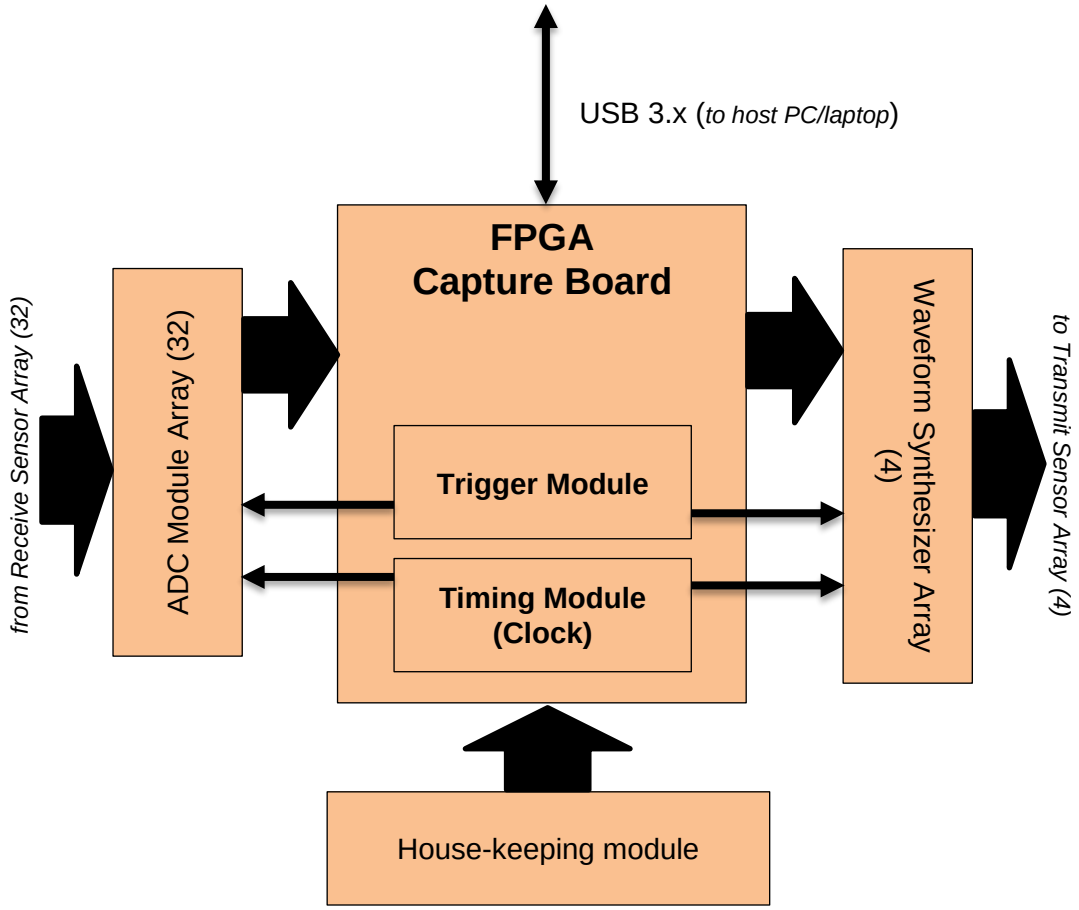

Fig. 1: Block diagram of proposed high-speed data acquisition system.

4 PROPOSAL SPECIFICATION

All proposals are to be submitted in a format specified in this enquiry (if applicable). However, tenderers are welcome to submit additional / alternative proposals over and above the originally specified format.

System Overview

The block diagram of the required system is shown in Fig. 1. The scope of work for the proposed solution shall include:

A. ADC Module Array

The ADC module array will consist of up to 32 ADC modules. All modules must be synchronized simultaneously by the falling-edge of the trigger pulse which will be

generated by the trigger module. Each module may consist of a minimum of 2 or maximum of 8 channels. Each channel (Fig. 2) is made up of a pre-amplifier stage followed by an analogue to digital conversion stage in the following order:

i. Fixed-gain, low noise amplifier (LNA): Differential-to-differential LNA with a fixed gain of 20 dB and an operating bandwidth of at least 1 MHz.

ii. Variable gain amplifier (VGA): consisting of a programmable attenuator with selectable attenuation of -40 dB or 0 dB; and a programmable fixed-gain amplifier with 5 selectable gains between 0 and 30 dB.

iii. Anti-aliasing filter (AAF):
- Programmable third-order low pass filter (LPF) with selectable cut-off of 500 kHz and 1 MHz
- Third-order high pass filter (HPF) with a fixed cut-off of 5 kHz.
- Stopband attenuation: -100 dB.

iv. Analogue-to-digital converter (ADC):
- Differential input voltage range: ±1.25 V (2.5 V_{p-p}).
- Sampling resolution: 16-bit (>14-bit effective)
- Sampling rate: configurable in octave steps between 31.25 kSPS and 2 MSPS (i.e. 31.25 kSPS, 62.5 kSPS, 125 kSPS, 250 kSPS, 500 kSPS, 1 MSPS, 2 MSPS)
- Appropriate digital signalling method
- Triggering: falling-edge triggering

v. Differential analogue output (ADC by-pass) connector

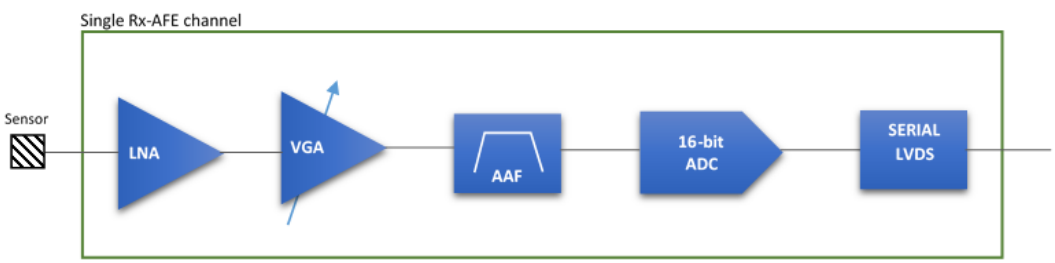

Fig. 2 Single-channel receiver analogue front-end

B. Waveform Synthesizer Array

The Waveform Synthesizer array will consist of 4 channels. Each channel must convert a digitally-defined waveform to an analogue signal to be applied to the transmit sensor array

on the rising edge of the trigger pulse generated by the trigger module. Each channel (Fig. 3) must consist of the following:

i. Arbitrary waveform generator with a FIFO buffer size of between 32678 and 2M samples to store and generate a digitally-specified waveform. The digital waveform will be generated from the host PC/laptop.

ii. Digital-to-analogue converter (DAC)
   - Resolution: 16-bit (>14-bit effective)
   - Update rate: configurable in octave steps between 31.25 kSPS and 2 MSPS (i.e. 31.25 kSPS, 62.5 kSPS, 125 kSPS, 250 kSPS, 500 kSPS, 1 MSPS, 2 MSPS)
   - Output voltage range: ± 5V (10 V_{p-p})
   - Single-ended output

iii. Op-amp driver: power amplifier single-ended input impedance – 1 kOhms (Apex MP108 Power amplifier)

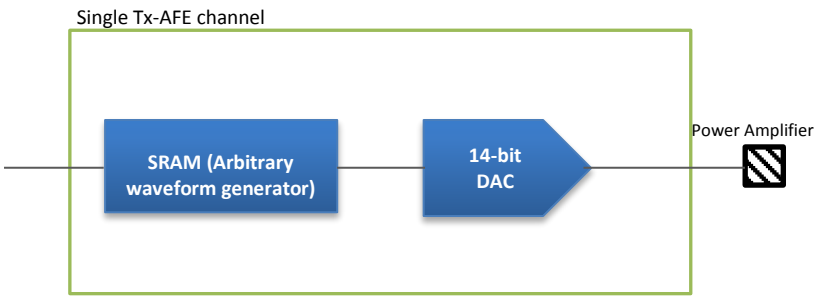

Fig. 3 Single-channel transmit analogue front-end

C. Trigger Module

The trigger module must produce configurable trigger pulses to synchronize the transmission and reception of signals on the system and any other similar system for expanded capability. The parameters of the trigger pulse will be supplied from the control platform (laptop/PC). The typical timing diagram of the trigger pulse illustrating the configurable parameters of the trigger are shown in Fig. 4 below. The waveform synthesizing (transmission) must occur on the rising edge of the pulse, while acquisition (sampling) must occur on the falling edge of the pulse.

Two trigger modes are required:

- Auto-generation mode: in this mode, the trigger module will on command continuously generate the trigger waveform until such a time that the command to stop triggering is received.
- Controlled (software triggering) mode: in this mode the trigger module must generate a single trigger pulse only when given a software trigger from the host PC/laptop.

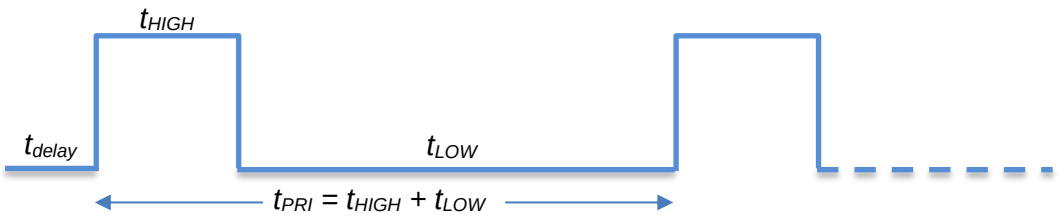

Fig 4. Trigger diagram showing configurable parameters. The trigger module must be able to generate the pulses to within a tenth (1/10) of a wavelength i.e. within 160 nanoseconds. The minimum duration of t_{HIGH} is 3 milliseconds. The maximum duration of t_{LOW} is 800 milliseconds. Note: t_{delay} = 1 millisecond (default) must occur only once at the start of the trigger pulse train.

D. Timing (Clock) Module

The timing module will generate low-noise, low-jitter clock signal necessary to achieve the sampling and generation rates required. The timing module must be phase aligned to a tenth-wavelength to support cascading of multiple systems. The timing module should be able to provide configurable data acquisition and generation rates across all channels simultaneously in octave steps between 31.25 kHz and 2 MHz (i.e. 31.25 kHz, 62.5 kHz, 125 kHz, 250 kHz, 500 kHz, 1 MHz, 2 MHz).

E. FPGA Capture Board

The capture board shall coordinate/control all acquisition and generation operations as well as stream all acquired data primarily over USB 3.x interface to a PC/laptop. This board must be capable of and/or facilitate the following:

i. Timing (clock) generation as described above
ii. Trigger generation as described above including
    - Pulse repetition frequency: 10 Hz (typical)
iii. Simultaneous capture (ADC)

- Number of channels: 32 channels (typical)
- Sampling mode: Finite samples
- Number of samples per channel: 250 kS (typical); 500 kS (maximum)
- Sampling rate: configurable in octave steps between 31.25 kSPS and 2 MSPS (i.e. 31.25 kSPS, 62.5 kSPS, 125 kSPS, 250 kSPS, 500 kSPS, 1 MSPS, 2 MSPS)
- Resolution: 16-bit (>14-bit effective)
- Capture rate: 10 Hz (typical)

iv. Simultaneous generation/waveform synthesis (DAC):

- Number of channels: 4 channels
- Generation mode: finite samples, regenerative mode (i.e. unless new digital waveforms are specified, previously generated waveforms are repeatedly transmitted)
- Number of samples per channel: 32 kS (typical); 2 MS (max)
- Update rate: configurable in octave steps between 31.25 kSPS and 2 MSPS (i.e. 31.25 kSPS, 62.5 kSPS, 125 kSPS, 250 kSPS, 500 kSPS, 1 MSPS, 2 MSPS)
- Resolution: 16-bit (>14-bit effective)
- Generation rate (pulse repetition frequency): 10 Hz (typical)

v. High-speed data stream over the One (1) Active USB 3.x. The board must also be capable of streaming over One (1) 1 Gigabit Ethernet but not necessarily functional at the time of delivery of the system

vi. High-speed data port (32 x 100 MHz) for high-throughput data streaming.

F. Firmware and Application Programming Interface (API):

The FPGA firmware/software and C/C++ libraries for controlling the acquisition, generation and streaming process shall be developed together with all supporting documentation. The system shall be controlled by user commands which will include but not be limited to the following:

i. Acquisition Configuration

- Acquisition task creation: acquisition task name, task ID, etc.
- Acquisition task deletion
- Channel select: list of channels to be used in acquisition

- AFE configuration
    - Variable gain select: a tuple or array thereof consisting {*channel id, gain select*}
    - LPF cut-off select: a tuple or array thereof consisting {*channel id, LPF cut-off*}
- ADC configuration
    - Number of samples per channel (all selected channel)
    - Trigger edge configuration (all selected channels): rising edge (0) or falling edge (1).
    - Sampling rate (all selected channels): 2 MSPS (typical). Adjustable range: 31.25 kHz, 62.5 kHz, 125 kHz, 250 kHz, 500 kHz, 1 MHz, 2 MHz
- Start/Stop acquisition
- Read samples

ii. Generation configuration

- Generation task creation: generation task name, task ID, etc.
- Generation task deletion.
- Channel select: list of channels to be used in generation
- Digital waveform per channel: digital waveform for each channel.
- Waveform sampling rate (all selected channels): 2 MSPS (typical). Adjustable range: 31.25 kHz, 62.5 kHz, 125 kHz, 250 kHz, 500 kHz, 1 MHz, 2 MHz
- Trigger edge configuration (all selected channels): rising edge (0) or falling edge (1).
- Start/Stop generation

iii. Trigger

- Trigger task name
- Trigger mode: 0 = Auto-generation; 1 = Controlled
- Trigger parameters: t_{delay}, t_{HIGH}, t_{LOW}

G. House-keeping module for operational information such as voltage and current readings, pressure sensors, leakage (moisture) sensor, etc.

H. All documentation including but not limited to all CAD files, PCB design files, BOM, schematics, source code (FPGA HDL files, C/C++ libraries).

I. Operating manual including calibration report of transmit and receive analogue front end specifying all AC specifications, Digital specifications, Switching specifications, ADC timing diagrams, Pin configurations and descriptions, typical performance characteristic graphs and absolute maximum ratings.

J. Size requirements: the system is required to fit into an enclosure consisting of two compartments separated by about 310mm. Each compartment measures about 258 mm (L) by 98 mm (W) by 50 mm (H).

5 FUNCTIONAL EVALUATION CRITERIA

5.1 The evaluation of the functional / technical detail of the proposal will be based on the following criteria:

Criteria	Weighting
A proven track record of high-speed (high data rate) multi-channel simultaneous data acquisition and generation system design and development.	25%
A proven track record of design and development of FPGA-based embedded system including FPGA programming and firmware development.	20%
A proven track record in electronic product development including professional, high-density surface mount PCB mechanical and electrical design and manufacturing.	10%
A proven track record of designing ultra-low noise and high sensitivity analogue circuitry including EMC design as well as screening.	5%
A proven track record in sonar/radar transceiver system design	10%
A proven track record of design and development of low phase noise frequency synthesizer and coherent clock distribution system.	10%
A proven track record of software/application programming interface (API) development in C/C++	5%
Commenting on (within their proposal) the ease of this product development and functionality and/or possible complications of the	5%

required specifications and its development.	
Warranty and maintenance of delivered system	5%
Delivery timescale	5%

5.2 Proposals with functionality/technical points of less than the pre-determined minimum overall percentage of 70% will be eliminated from further evaluation.

5.3 Refer to Annexure A for the scoring sheet that will be used to evaluate functionality**.**

6 ELIMINATION CRITERIA

Proposals will be eliminated under the following conditions:

- Submission after the deadline;
- Proposals submitted at incorrect location; and
- Non-attendance of the compulsory briefing session / site inspection.
- Proposed system does not fit into enclosure with specified dimensions.

7 NATIONAL TREASURY CENTRAL SUPPLIER DATABASE REGISTRATION

Before any negotiations will start with the winning bidder it will be required from the winning bidder to:

- be registered on National Treasury's Central Supplier Database (CSD). Registrations can be completed online at: www.csd.gov.za;
- provide the CSIR of their CSD registration number; and

provide the CSIR with a certified copy of their B-BBEE certificate. If no certificate can be provided, no points will be scored during the evaluation process. (RSA suppliers only)

SECTION B – TERMS AND CONDITIONS

8 VENUE FOR PROPOSAL SUBMISSION

All proposals must be submitted at:

- **CSIR GATE 03 - Main Reception Area** (in the **Tender box**) at the following address

  Council for Scientific and Industrial Research (CSIR)
  Meiring Naudé Road
  Brummeria
  Pretoria

9 TENDER PROGRAMME

The tender program, as currently envisaged, incorporates the following key dates:

• Issue of tender documents:	16 August 2019
• Compulsory briefing session / site inspection etc:	23 August 2019
• Closing / submission Date:	02 September 2019
• Estimate appointment date of successful tenderer:	20 September 2019
• Estimated contract duration (in months/years)	6 months

10 SUBMISSION OF PROPOSALS

10.1 All proposals are to be sealed. No open proposals will be accepted.

10.2 All proposals are to be clearly marked with the RFP number and the name of the tenderer on the outside of the main package. Proposals must consist of two parts, each of which is placed in a separate sealed package clearly marked:

PART 1: Technical Proposal: RFP No.: 892/02/09/2019

PART 2: Pricing Proposal, Delivery Milestones and Timescales (Gant Chart), B-BBEE and other Mandatory Documentation:

RFP No.: 892/02/09/2019

10.3 Proposals submitted by companies must be signed by a person or persons duly authorised.

10.4 The CSIR will award the contract to qualified tenderer(s)' whose proposal is determined to be the most advantageous to the CSIR, taking into consideration the technical (functional) solution, price and B-BBEE.

11 DEADLINE FOR SUBMISSION

Proposals shall be submitted at the address mentioned above no later than the closing date of ***Monday, 02 September 2019*** during CSIR's business hours. The CSIR business hours are between 08h00 and 16h30.

Where a proposal is not received by the CSIR by the due date and stipulated place, it will be regarded as a late tender. Late tenders will not be considered.

12 AWARDING OF TENDERS

12.1 Awarding of tenders will be published on the CSIR's tender website. No regret letters will be sent out.

13 EVALUATION PROCESS

13.1 Evaluation of proposals

All proposals will be evaluated by an evaluation team for functionality, price and B-BBEE. Based on the results of the evaluation process and upon successful negotiations, the CSIR will approve the awarding of the contract to successful tenderers.

A two-phase evaluation process will be followed.

- The first phase includes evaluation of **elimination** and **functionality criteria**, local production and content.
- The second phase includes the evaluation of **price** and **B-BBEE** status.

Pricing Proposals will only be considered after functionality phase has been adjudicated and accepted. Only proposals that achieved the specified minimum qualification scores for functionality will be evaluated further using the preference points system.

13.2 Preference points system

The 80/20 preference point system will be used where 80 points will be dedicated to price and 20 points to B-BBEE status. If all tenders received are more than R50m, the proposal will be cancelled and re-issued.

PRICING PROPOSAL

13.3 Pricing proposal must be cross-referenced to the sections in the Technical Proposal. Any options offered must be clearly labelled. Separate pricing must be provided for each option offered to ensure that pricing comparisons are clear and unambiguous.

13.4 Price needs to be provided in South African Rand (excl. VAT), with details on price elements that are subject to escalation and exchange rate fluctuations clearly indicated.

13.5 Price should include additional cost elements such as freight, insurance until acceptance, duty where applicable.

13.6 Only firm prices* will be accepted during the tender validity period. Non–firm prices** (including prices subject to rates of exchange variations) will not be considered.

**Firm price is the price that is only subject to adjustments in accordance with the actual increase or decrease resulting from the change, imposition, or abolition of customs or excise duty and any other duty, levy, or tax which, in terms of a law or regulation is binding on the contractor and demonstrably has an influence on the price of any supplies, or the rendering costs of any service, for the execution of the contract;*

***Non-firm price is all prices other than "firm" prices.*

13.7 Payment will be according to the CSIR Payment Terms and Conditions.

14 VALIDITY PERIOD OF PROPOSAL

Each **proposal** shall be valid for a minimum period of three (3) months calculated from the closing date.

15 APPOINTMENT OF SERVICE PROVIDER

15.1 The contract will be awarded to the tenderer who scores the highest total number of points during the evaluation process, except where the law permits otherwise.

15.2 Appointment as a successful service provider shall be subject to the parties agreeing to mutually acceptable contractual terms and conditions. In the event of the parties failing to reach such agreement CSIR reserves the right to appoint an alternative supplier.

15.3 Awarding of contracts will be announced on the National Treasury website and no regret letters will be sent to unsuccessful bidders.

16 ENQUIRIES AND CONTACT WITH THE CSIR

Any enquiry regarding this RFP shall be submitted in writing to CSIR at tender@csir.co.za with "RFP No 892/02/09/2019 - The provision for the design and production of a Transceiver Analogue Front End and High Speed Digital Data Capture System to CSIR" as the subject.

Any other contact with CSIR personnel involved in this tender is not permitted during the RFP process other than as required through existing service arrangements or as requested by the CSIR as part of the RFP process.

17 MEDIUM OF COMMUNICATION

All documentation submitted in response to this RFP must be in English.

18 COST OF PROPOSAL

Tenderers are expected to fully acquaint themselves with the conditions, requirements and specifications of this RFP before submitting proposals. Each tenderer assumes all risks for resource commitment and expenses, direct or indirect, of proposal preparation and participation throughout the RFP process. The CSIR is not responsible directly or indirectly for any costs incurred by tenderers.

19 CORRECTNESS OF RESPONSES

19.1 The tenderer must confirm satisfaction regarding the correctness and validity of their proposal and that all prices and rates quoted cover all the work/items specified in the RFP. The prices and rates quoted must cover all obligations under any resulting contract.

19.2 The tenderer accepts that any mistakes regarding prices and calculations will be at their own risk.

20 VERIFICATION OF DOCUMENTS

20.1 Tenderers should check the numbers of the pages to satisfy themselves that none are missing or duplicated. No liability will be accepted by the CSIR in regard to anything arising from the fact that pages are missing or duplicated.

20.2 *One hard copy and one electronic copy (CD or USB memory key)* of each proposal must be submitted. In the event of a contradiction between the submitted copies, the hard copy shall take precedence.

20.3 Pricing schedule and B-BBEE credentials should be submitted with the proposal, but as a separate document and no such information should be available in the technical proposal.

20.4 If a courier service company is being used for delivery of the proposal document, the RFP description must be endorsed on the delivery note/courier packaging to ensure that documents are delivered to the tender box, by the stipulated due date.

21 SUB-CONTRACTING

21.1 A tenderer will not be awarded points for B-BBEE status level if it is indicated in the tender documents that such a tenderer intends sub-contracting more than **25%** of the value of the contract to any other enterprise that does not qualify for at least the points that such a tenderer qualifies for, unless the intended sub-contractor is an exempted micro enterprise that has the capability and ability to execute the sub-contract.

21.2 A tenderer awarded a contract may not sub-contract more than **25%** of the value of the contract to any other enterprise that does not have an equal or higher B-BBEE status

level than the person concerned, unless the contract is sub-contracted to an exempted micro enterprise that has the capability and ability to execute the sub-contract.

22 ENGAGEMENT OF CONSULTANTS

The consultants will only be remunerated at the rates:

22.1 Determined in the "Guideline for fees", issued by the South African Institute of Chartered Accountants (SAICA); or

22.2 Set out in the "Guide on Hourly Fee Rates for Consultants", by the Department of Public Service and Administration (DPSA); or

22.3 Prescribed by the body - regulating the profession of the consultant.

23 TRAVEL EXPENSES

23.1 All travel expenses for the CSIR's account, be it directly via the CSIR's travel agent or indirectly via re-imbursements, must be in line with the CSIR's travel policy. The following will apply:

23.1.1 Only economy class tickets will be used.

23.1.2 A maximum of R1300 per night for accommodation, dinner, breakfast and parking will be allowed.

23.1.3 No car rentals of more than a Group B will be accommodated.

24 ADDITIONAL TERMS AND CONDITIONS

24.1 A tenderer shall not assume that information and/or documents supplied to CSIR, at any time prior to this request, are still available to CSIR, and shall consequently not make any reference to such information document in its response to this request.

24.2 Copies of any affiliations, memberships and/or accreditations that support your submission must be included in the tender.

24.3 In case of proposal from a joint venture, the following must be submitted together with the proposal:

- Joint venture Agreement including split of work signed by both parties;
- The original or certified copy of the B-BBEE certificate of the joint venture;

- The Tax Clearance Certificate of each joint venture member;
- Proof of ownership/shareholder certificates/copies; and
- Company registration certificates.

24.4 An omission to disclose material information, a factual inaccuracy, and/or a misrepresentation of fact may result in the disqualification of a tender, or cancellation of any subsequent contract.

24.5 Failure to comply with any of the terms and conditions as set out in this document will invalidate the Proposal.

25 CSIR RESERVES THE RIGHT TO

25.1 Extend the closing date;

25.2 Verify any information contained in a proposal;

25.3 Request documentary proof regarding any tendering issue;

25.4 Give preference to locally manufactured goods;

25.5 Appoint one or more service providers, separately or jointly (whether or not they submitted a joint proposal);

25.6 Award this RFP as a whole or in part;

25.7 Cancel or withdraw this RFP as a whole or in part.

26 DISCLAIMER

This RFP is a request for proposals only and not an offer document. Answers to this RFP must not be construed as acceptance of an offer or imply the existence of a contract between the parties. By submission of its proposal, tenderers shall be deemed to have satisfied themselves with and to have accepted all Terms & Conditions of this RFP. The CSIR makes no representation, warranty, assurance, guarantee or endorsements to tenderer concerning the RFP, whether with regard to its accuracy, completeness or otherwise and the CSIR shall have no liability towards the tenderer or any other party in connection therewith.

DECLARATION BY TENDERER

Only tenderers who completed the declaration below will be considered for evaluation.

RFP No: 892/02/09/2019

I hereby undertake to render services described in the attached tendering documents to CSIR in accordance with the requirements and task directives / proposal specifications stipulated in RFP No: **892/02/09/2019** at the price/s quoted. My offer/s remains binding upon me and open for acceptance by the CSIR during the validity period indicated and calculated from the closing date of the proposal.

I confirm that I am satisfied with regards to the correctness and validity of my proposal; that the price(s) and rate(s) quoted cover all the services specified in the proposal documents; that the price(s) and rate(s) cover all my obligations and I accept that any mistakes regarding price(s) and rate(s) and calculations will be at my own risk.

I accept full responsibility for the proper execution and fulfilment of all obligations and conditions devolving on me under this proposal as the principal liable for the due fulfilment of this proposal.

I declare that I have no participation in any collusive practices with any tenderer or any other person regarding this or any other proposal.

I accept that the CSIR may take appropriate actions, deemed necessary, should there be a conflict of interest or if this declaration proves to be false.

I confirm that I am duly authorised to sign this proposal.

NAME (PRINT) …….

CAPACITY ……..

SIGNATURE …….

NAME OF FIRM ……..….

DATE ……

WITNESSES

1 ……

2 ……

DATE:……..

27 ANNEXURE A

Criteria	Weighting	0	7	10
A proven track record of high-speed (high data rate) multi-channel simultaneous data acquisition and generation system design and development.	25%	No proof of a successful high-speed data acquisition system development with support for simultaneous multiple channel acquisition and generation	Proof of 1 – 2 successful high-speed data acquisition system(s) with support for simultaneous multiple channel acquisition and generation	Proof of at least 3 successful high-speed data acquisition system(s) with support for simultaneous multiple channel acquisition and generation
A proven track record of design and development of FPGA-based embedded system including FPGA programming and firmware development.	20%	No proof of a successful FPGA-based embedded system design and FPGA programming/firmware development.	Proof of 1 - 2 successful FPGA-based embedded system(s) with accompanying FPGA firmware.	Proof of at least 3 FPGA-based embedded system(s) with accompanying FPGA firmware. Full points will be awarded if at least one of the systems is an ALTERA/Intel based system
A proven track record in electronic product development including professional, high-density surface mount PCB mechanical and electrical design and manufacturing.	10%	No proof of a successful electronic product development.	Proof of 1 - 2 successful electronic product development including professional, high-density surface mount PCB mechanical and electrical design and manufacturing.	Proof of at least 3 successful electronic product developments including professional, high-density surface mount PCB mechanical and electrical design and manufacturing.
A proven track record of designing ultra-low noise and high sensitivity analogue circuitry including EMC design as well as screening.	5%	No proof of successful ultra-low noise, high-sensitivity analogue circuitry with EMC and screening.	Proof of 1 – 2 successful ultra-low noise, high-sensitivity analogue circuitry with EMC and screening.	Proof of at least 3 successful ultra-low noise, high-sensitivity analogue circuitry with EMC and screening.
A proven track record in sonar/radar transceiver system design	10%	No proof of successful sonar/radar transceiver	Proof of 1 – 2 sonar/radar transceiver	Proof of at least 3 sonar/radar transceiver

		system design.	system design.	system design.
A proven track record of design and development of low phase noise frequency synthesizer and coherent clock distribution system.	10%	No proof of successful development of low phase noise frequency synthesizer and coherent clock distribution system.	Proof of 1 - 2 successful development of low phase noise frequency synthesizer and coherent clock distribution system.	Proof of at least 3 successful developments of low phase noise frequency synthesizer and coherent clock distribution system.
A proven track record of software/application programming interface (API) development in C/C++	5%	No proof of successful software/application programming interface development in C/C++.	Proof of 1 – 2 successful software/application programming interface development in C/C++.	Proof of at least 3 successful software/application programming interface development in C/C++.
Commenting on (within their proposal) the ease of this product development and functionality and/or possible complications of the required specifications and its development.	5%	No technically valid and/or value adding and/or non-obvious (to those in the field) point are mentioned. As adjudged by the evaluation panel	2 - 3 technically valid and/or value adding and/or non-obvious (to those in the field) points are mentioned. As adjudged by the evaluation panel. Seven (7) for mentioning three valid points	At least 4 or more technically valid and/or value adding and/or non-obvious (to those in the field) points are mentioned. As adjudged by the evaluation panel. Eight (8) for mentioning 4 - 5 valid points. Nine (9) for mentioning 6 – 8 valid points. Ten (10) for mentioning 9 or more points.
Warranty and maintenance of delivered system	5%	No warranty and maintenance plan	Less than 3 year warranty and maintenance plan	4 year warranty and maintenance plan
Delivery timescale	5%	Delivery after 31 January 2020	Delivery on/before 31 January 2020	Delivery on/before 1 January 2020